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PRE-APPEAL BRIEF REQUEST FOR REVIEW

Docket Number (Optional)
MTKP0118USA

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on 05/30/2008

Signature Alex Liang

Typed or printed name Alex Liang

Application Number	Filed
10/709,551	05/13/2004

First Named Inventor
Yao-Jen Liang

Art Unit	Examiner
2182	VIDWAN, JASJIT S

Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request.

This request is being filed with a notice of appeal.

The review is requested for the reason(s) stated on the attached sheet(s).
Note: No more than five (5) pages may be provided.

I am the

☐ applicant/inventor.

☐ assignee of record of the entire interest.
See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed.
(Form PTO/SB/96)

☑ attorney or agent of record.
Registration number 41,526.

☐ attorney or agent acting under 37 CFR 1.34.
Registration number if acting under 37 CFR 1.34 _____

Winston Hsu
Signature

Winston Hsu
Typed or printed name

302-729-1562
Telephone number

05/30/2008
Date

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required.
Submit multiple forms if more than one signature is required, see below*.

☐ *Total of _____ forms are submitted.

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METHOD FOR TRANSMITTING DATA IN A MULTI-CHIP SYSTEM

Appl. No.	:	10/709,551	Confirmation No. 3550
Applicant	:	Yao-Jen Liang, Ming-Yang Chao	
Filed	:	May 13, 2004	
TC/A.U.	:	2182	
Examiner	:	VIDWAN, JASJIT S	
Docket No.	:	MTKP0118USA	
Customer No.	:	27765	

Commissioner for Patents
P.O. Box 1450
Alexandria VA 22313-1450

PRE-APPEAL BRIEF REQUEST FOR REVIEW

Reconsideration and allowance of claims 1-28 is respectfully requested because the independent method claim 1 and dependent apparatus claim 26 have been rejected based on an improper standard. Specifically, the Examiner's rejection of claim 1 relies on Fujii to teach claimed step (c) of the present invention, but then also states that it is "irrelevant" that Fujii's disclosed method of operation as a whole directly contradicts step (c) of the present invention. Additionally, dependent claims 2, 13, 14 and 24 have also been rejected based on an improper standard. Specifically, the Examiner did not provide reasonable motivation for combining the references in the way required by the rejection.

Concerning independent claim 1:

In the rejection of claim 1, the Examiner admits that the AAPA does not teach the following three features of the present invention (see sub-points a, b, and c on page 3 of the final Office action of 12/31/2007):

"(a) the slave chip informing the host chip of data needed to be transmitted;

(b) when being informed by the slave chip, the host chip informing the slave chip to start to transmit the data; and

(c) when being informed by the host chip, the slave chip starting to transmit the data to the host chip." (claim 1 – present invention)

The Examiner then refers to secondary reference Fujii et al. (US Patent # 5,898,695) and provides the following statements asserting that each of the above limitations not found in the AAPA are disclosed by Fujii (see also page 3 of the final Office action of 12/31/2007):

(a) "a transfer request signal "DREQ" is outputted…"

(b) "…transfer acknowledge signal DACK is sent back"

(c) "… and data is written in RAM without passing through the register of microprocessor"

In argument of point (c), in the applicant's response dated 03/17/2008, the applicant pointed out to the Examiner that "… and data is written in RAM without passing through the register of the microprocessor" taught by Fujii is not equivalent or similar to "the slave chip starting to transmit the data to the host chip", as is claimed in step (c) of claim 1 of the present invention. For instance, the microprocessor 12 is what generates the DACK signal and, therefore, microprocessor 12 must be interpreted by the Examiner to be the claimed host chip of the present invention. However, Fujii clearly teaches that "the data is written in RAM 7 without passing through the register of the microprocessor 12" (see column 6, lines 59-60 of Fujii et al.). In otherwords, Fujii et al. does not teach, and in fact contradicts, the claimed method step "(c) when being informed by the host chip, the slave chip starting to transmit the data to the host chip".

Additionally, in the applicant's response of 03/17/2008, the applicant pointed out that a person of ordinary skill in the art would not modify the AAPA to include the teachings of Fujii et al. to deduce the present invention because the teachings of Fujii are directed toward a direct memory access DMA operation of writing data directly from the transfer buffer 141 to the RAM 7 without passing through the microprocessor 12. This is in contrast to the present invention step stating, "(c) of when being informed by the host chip, the slave chip starting to transmit the data to the host chip".

Further comments indicating how a person of ordinary skill in the art having access to the AAPA, Fujii et al., and common sense would not deduce the present invention without further inventive process were also provided in the applicant's response of 10/08/2007. In particular, the Examiner appears to have simply found a reference (Fujii et

al.) that teaches some signals (DACK, DREQ, DATABUS, PACKET_DATA) being similar (but not the same) as the present invention, and then chose an improper reason why a person skilled in the art would take these signals out of the context of Fujii and somehow be combined with the AAPA to result in the present invention. The Examiner contends that all of this could be done without inventive process by the person skilled in the art, however, this is not fair to the applicant and does not follow proper 35 USC 103 rejections. The signals utilized in the context of Fujii's design do not have the same purpose or connection structure as claimed by the present invention; therefore, it would not obvious how to integrate them into the AAPA without further inventive process.

In response to applicant's arguments, the Examiner admitted in the advisory action of 04/17/2008, "Examiner humbly submits that had the Examiner only used the Fujii reference as either a sole reference [35 U.S.C 102] or as a primary reference in combinational rejection, Applicant's argument would be definitive." However, the Examiner then stated that "Examiner only relies on Fujii to teach the **method** of transferring data from one location to another without the necessity of providing a duplicate established structure of a host chip and a slave chip". More specifically, the Examiner emphasized in the same advisory action that "The actual functionality of each unit is irrelevant as the underlying structure was established using AAPA as a primary reference."

The applicant respectfully disagrees that the functionality of each unit of Fujii is irrelevant. In fact, it is very relevant because Fujii's method of transferring data from one location to another involves writing data in RAM 7 "without passing through the register of the microprocessor 12". That is, **Fujii is teaching a direct memory access DMA operation that directly contradicts one of the claimed limitations for which the Examiner is relying on Fujii.** Specifically, Fujii does not teach "the slave chip starting to transmit the data to the host chip", as is claimed in method step (c) of claim 1 of the present invention.

In summary, the applicant respectfully asserts it is not proper that the Examiner's rejection of claim 1 has relied on Fujii to teach claimed step (c) of the present invention, but then also states that it is "irrelevant" that Fujii's signals and method of operation directly contradict step (c) of the present invention.

A similar argument also applies to dependent apparatus claim 26, and claims 2-21

and 27-28 are dependent claims and should be found allowable for at least the same reasons. Additional comments regarding the rejections of particular dependent claims are provided in the below paragraphs.

Concerning dependent claims 2, 13, 14 and 24:

Applicant would also like to point out that the motivation to "provide a variable time-division multiplex communication method and apparatus in the system [see Satoh, Paragraph 0008]" as was stated by the Examiner in the Office action of 07/26/2007 does not have anything to do with the AAPA and Fujii. For one thing, Fujii would not benefit from including a time-division multiplex communication method. Furthermore, the present invention as claimed in claims 2, 13, 14, and 24 also does not include any such a system that would benefit from a time-devision multiplex communication method; therefore, this motivation is not proper. Similar to the rejections of claim 1 and 26, the Examiner appears to have chosen a motivation that simply would not have existed to a person skilled in the art at the time the invention was made.

The applicant points out that MPEP section 2143.01 states, "Obviousness can * be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so. In re Kahn, 441 F.3d 977, 986, 78 USPQ2d 1329, 1335 (Fed. Cir. 2006) (discussing rationale underlying the motivation-suggestion-teaching *>test< as a guard against using hindsight in an obviousness analysis). **" However, the Examiner did not provide a reasonable motivation that a person skilled in the art would understand to combine the references.

In summary, the Examiner did not provide reasonable motivation for combining the teachings of Satoh into the references of Fujii and the AAPA to thereby result in the present invention as claimed in claims 2, 13, 14, and 24 without further inventive process.

Conclusion:

Thus, all pending claims are submitted to be in condition for allowance with respect to the cited art for at least the reasons presented above. A pre-appeal brief conference to review the above arguments is respectfully requested.

Sincerely yours,

Winston Hsu

Date: May 30, 2008

Winston Hsu, Patent Agent No. 41,526

P.O. BOX 506, Merrifield, VA 22116, U.S.A.

Voice Mail: 302-729-1562

Facsimile: 806-498-6673

e-mail : winstonhsu@naipo.com

Note: Please leave a message in my voice mail if you need to talk to me. (The time in D.C. is 12 hours behind the Taiwan time, i.e. 9 AM in D.C. = 9 PM in Taiwan.)